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PSiP and PwrSoC Based Opportunities and Solutions for High Power Systems

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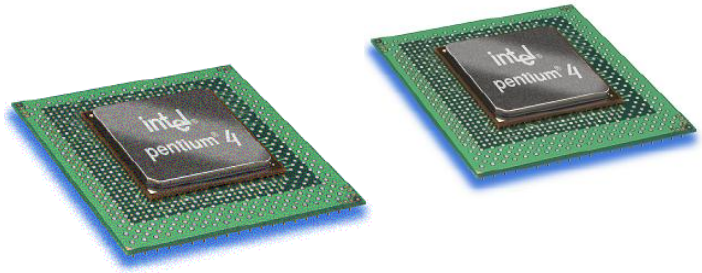
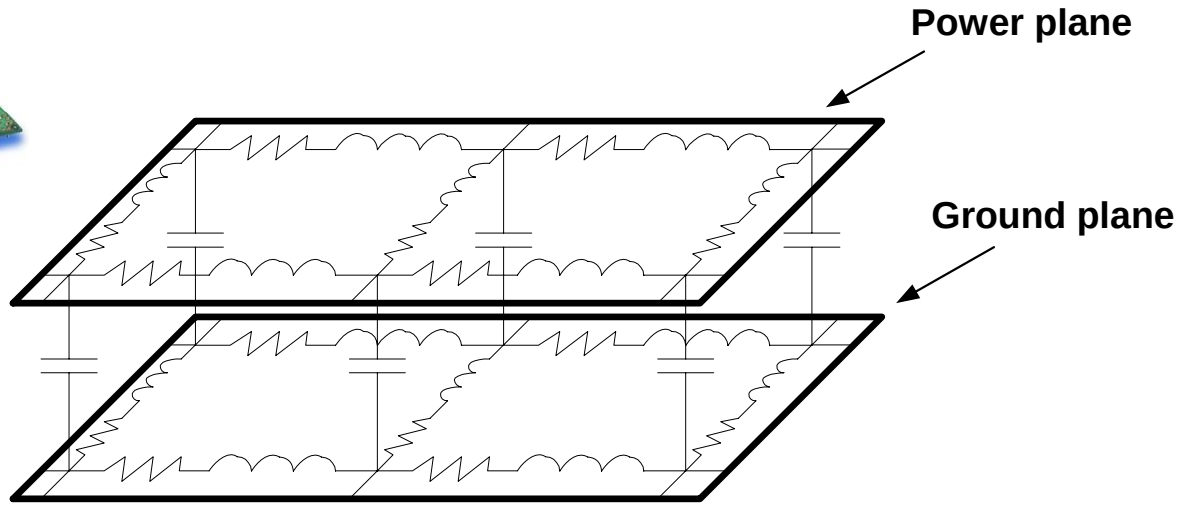
Outline

- Case 1: Powering Large Digital Processor ICs
- Case 2: Data Communication Power System
- Conclusion

Case 1: Powering Large Scale Digital ICs





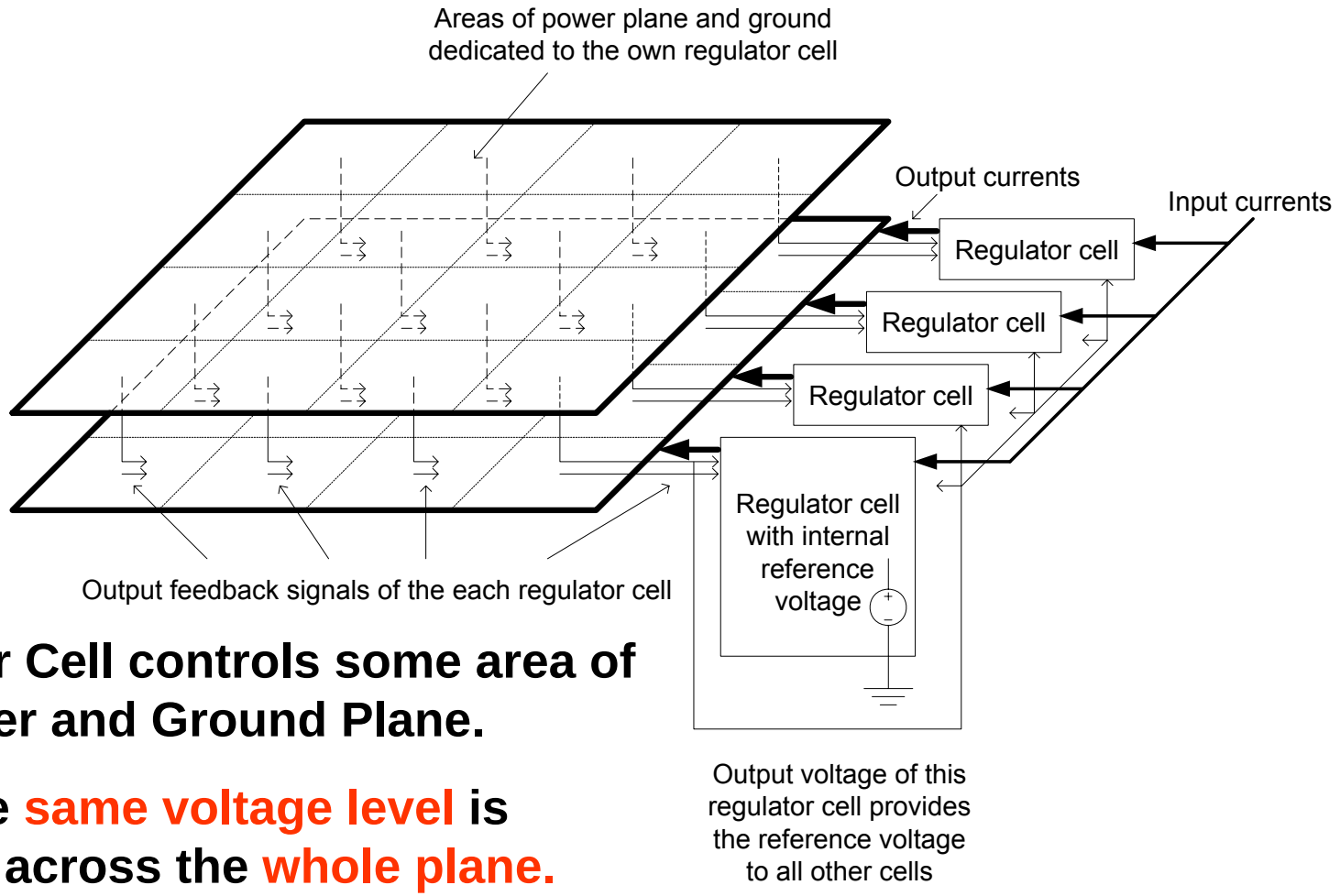
- **Power and Ground Planes provide supply voltage to large digital ICs**
- **Stray R, L and C of plane determine the voltage and current distribution.**
- **Existing Voltage Regulators control only one point of plane where the feedback is connected.**
- **All Power Distribution Area should have equal voltage potential for noise immunity and electromagnetic compatibility of digital system**

Note: This concept of powering large digital processors has been initially reported at ITS-2004 in presentation:

"Alternative Approach of Powering VLSI Digital ICs Using Multi-Cell VRM"

The related US Patent 6,646,425 has been awarded in 2003

Multi-Cell Voltage Regulator



Each Regulator Cell controls some area of the Power and Ground Plane.

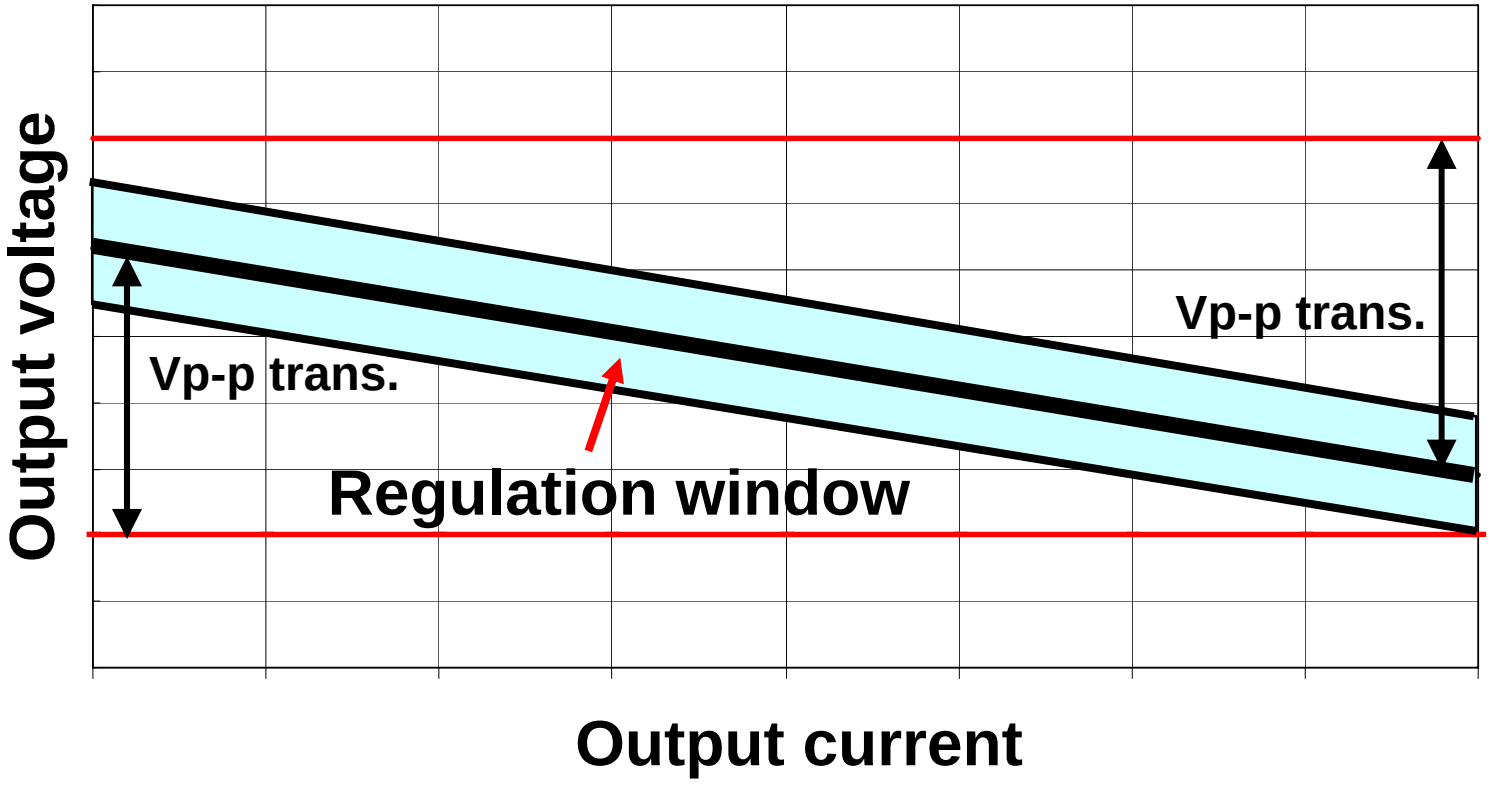
Thus, the same voltage level is maintained across the whole plane.

To avoid confusion: There is no physical separation of plane areas!

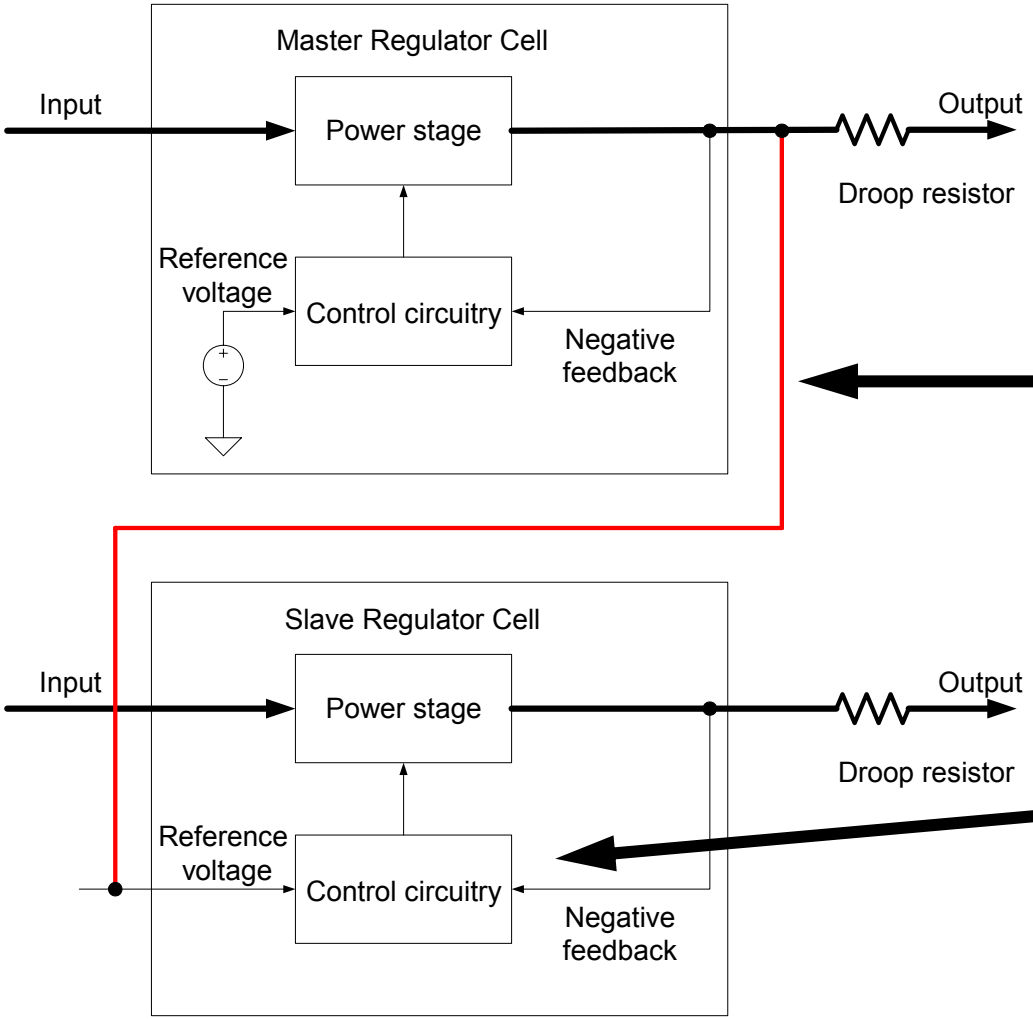
Load Line Regulation

"Load Line" type voltage regulation

- Improves performance and reliability of processor
- Provides wider window for the output voltage transients



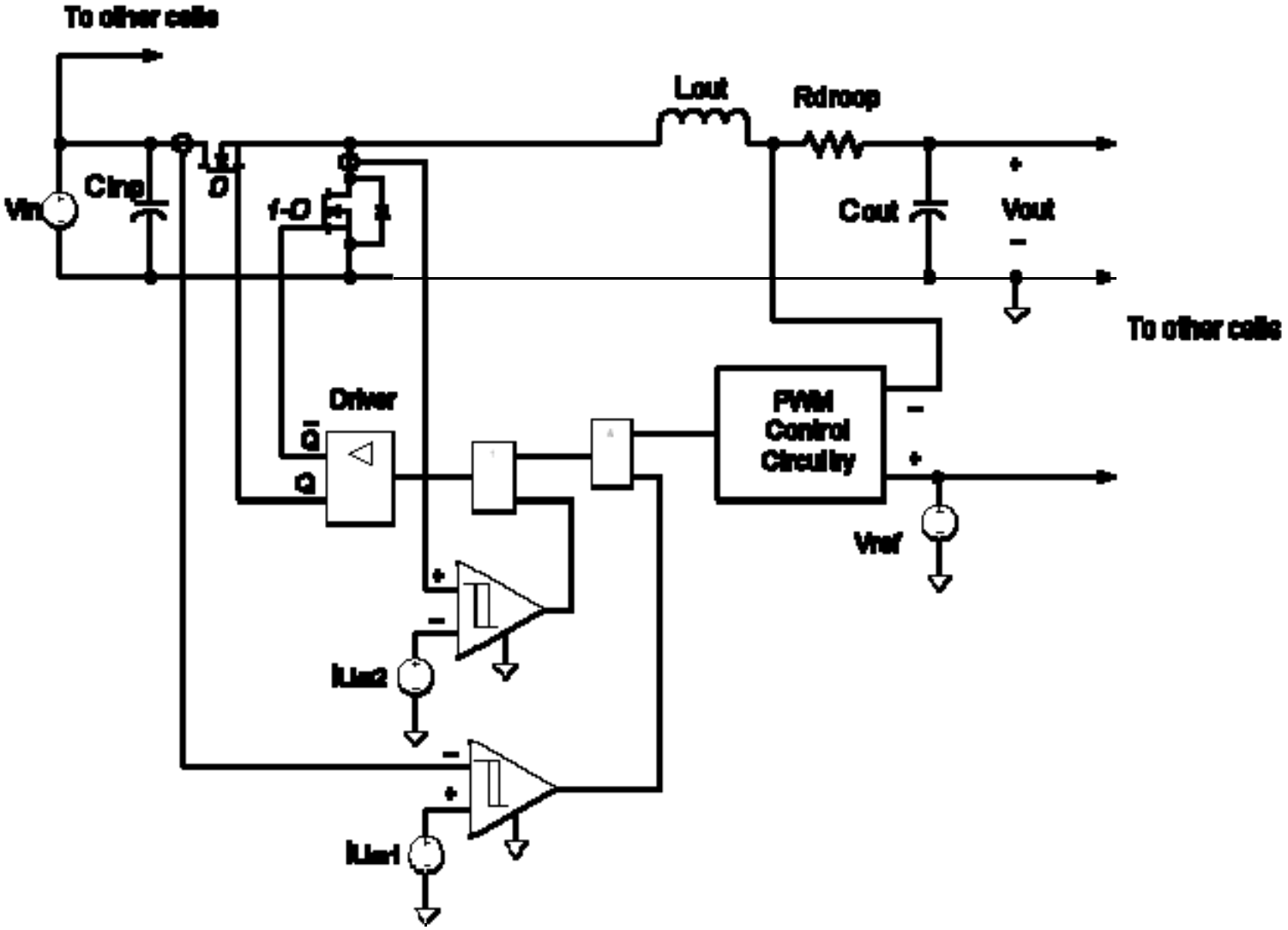
Modified Droop Paralleling Method



Output of one regulator is the reference voltage for another

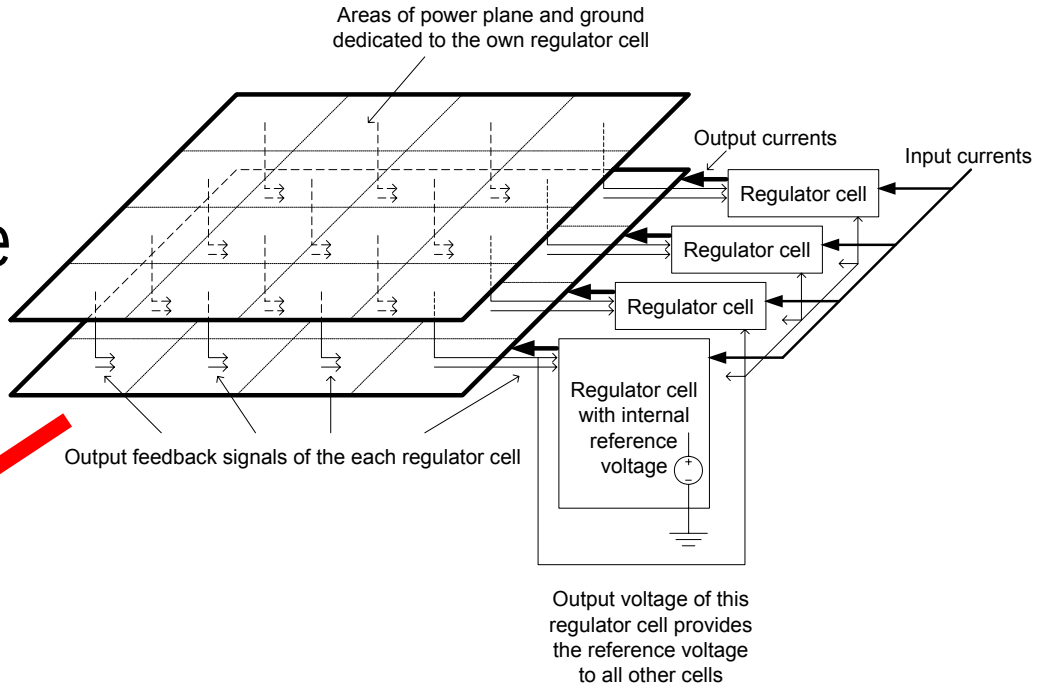
Offset is reduced to the level of Op. Amp. input offset

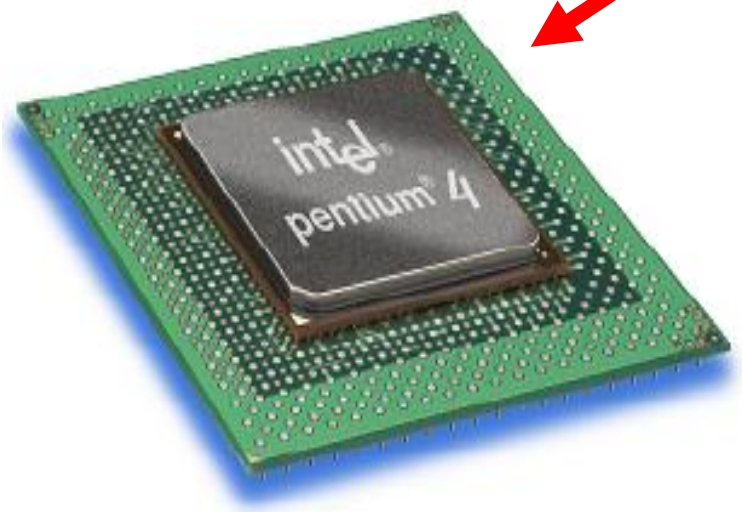
Implementation of Cell as Buck Converter



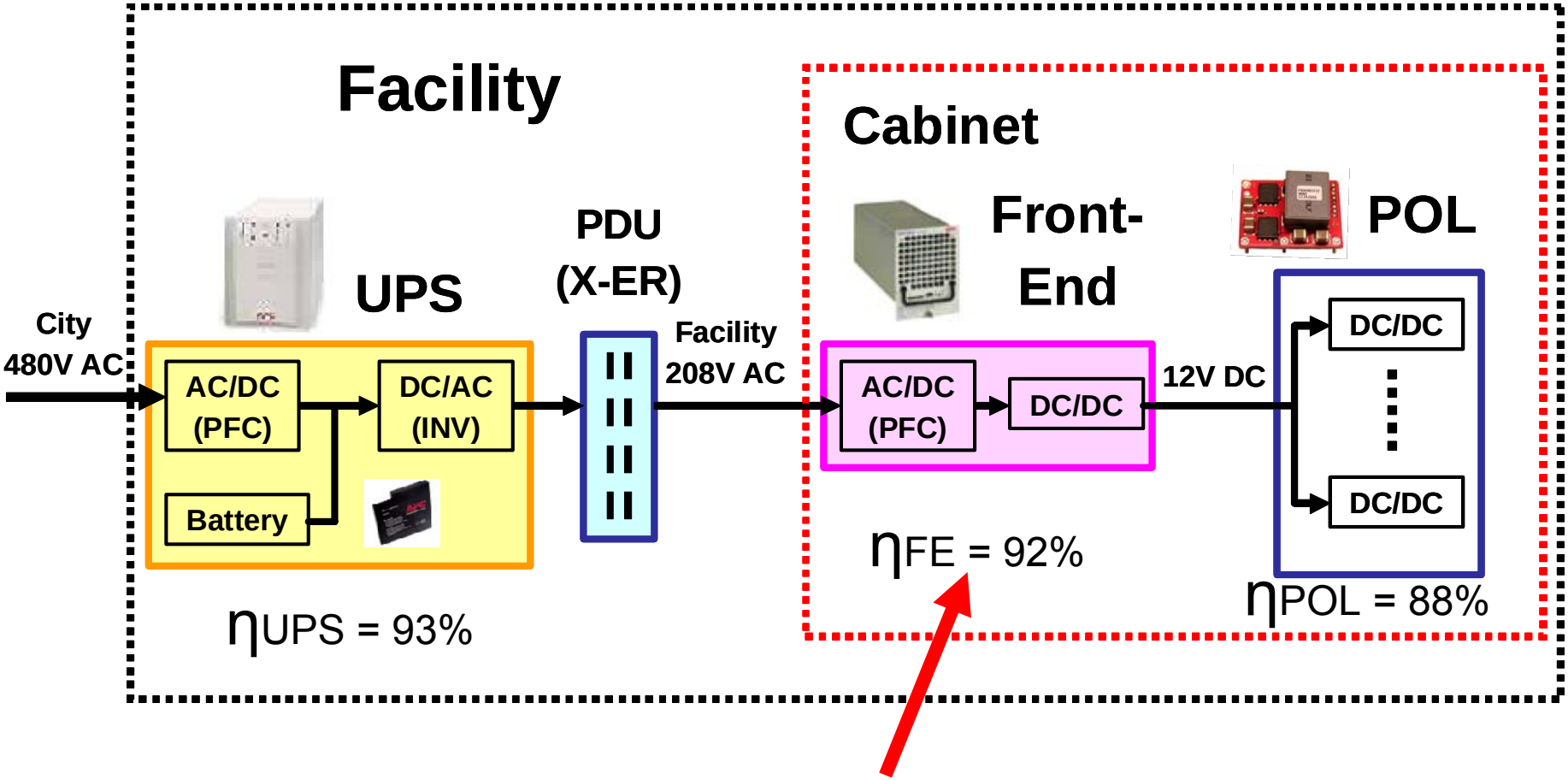
Next Integration Step

Such multi-cell power system can be integrated on the top of processor die inside the package



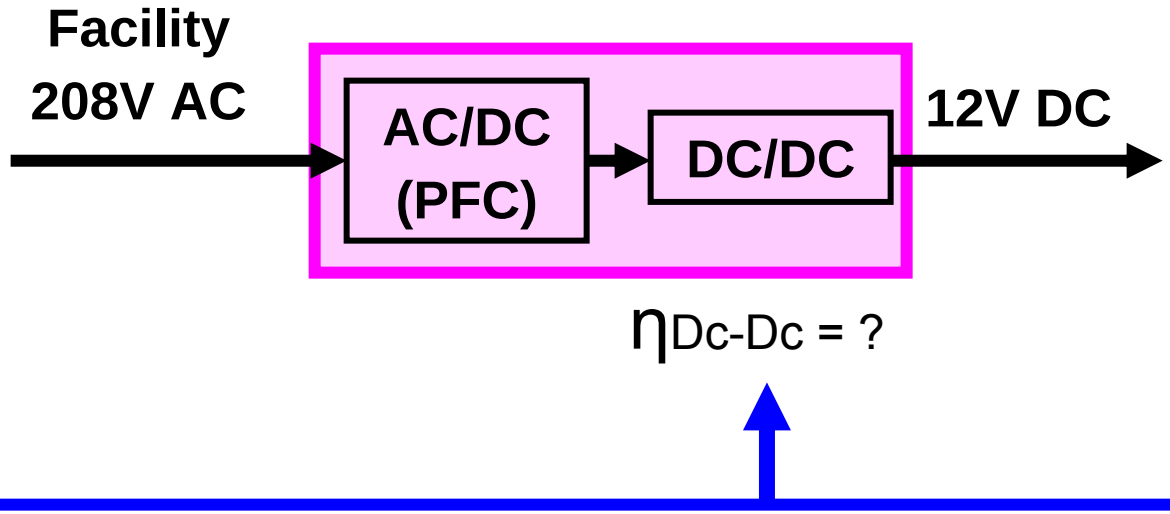


Case 2: Facility Power System with 208-V AC Distribution Bus



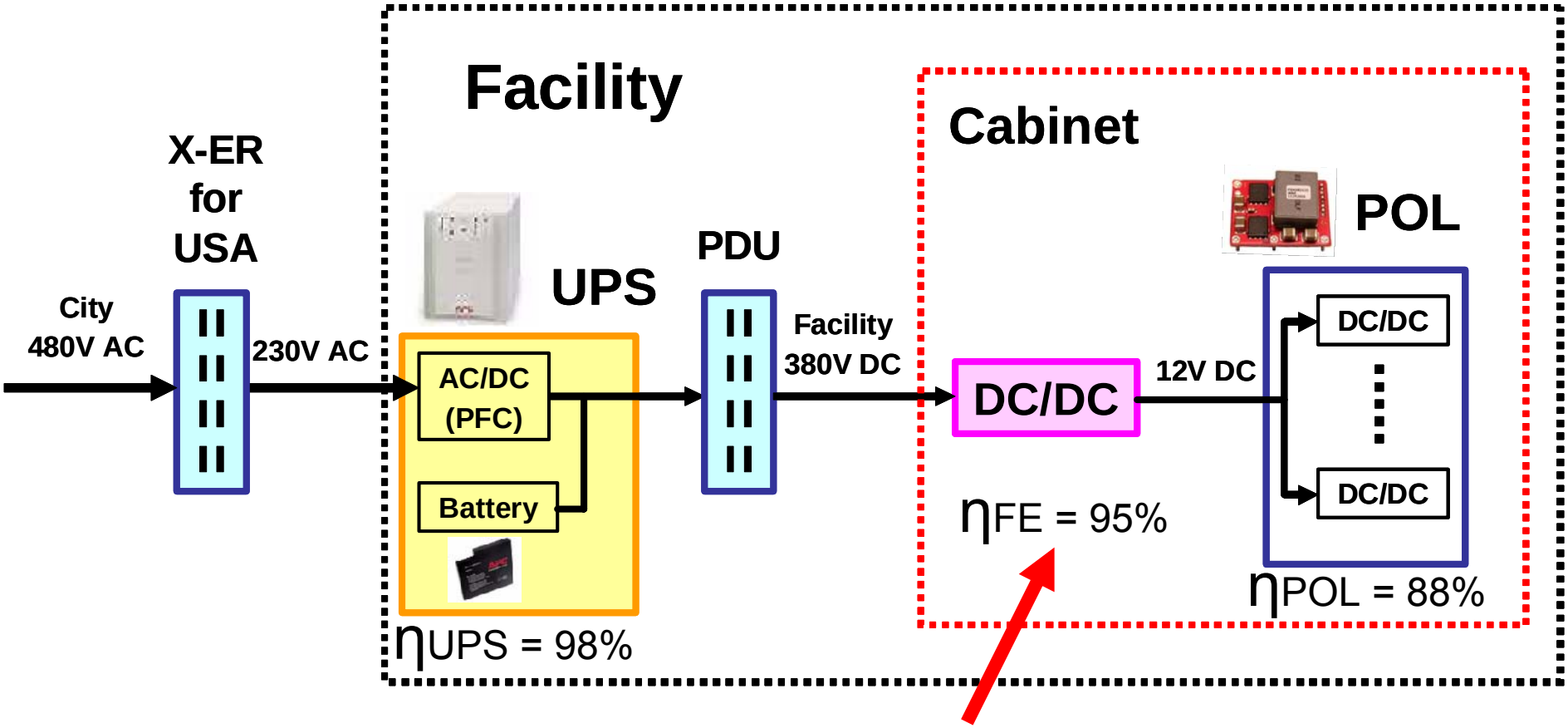
We consider demanding requirements to the Front-End Power Supply as part of such system

Design Goals for Dc-Dc Part of Front-End



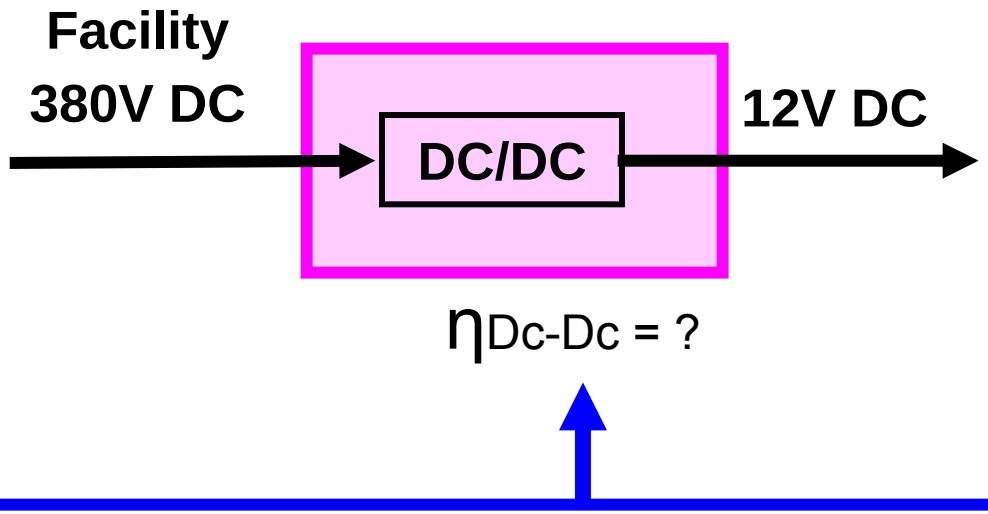
- Efficiency: 97% at half-load and 94.5% at full load
- Power Density: >40 W/cub.inch
- Cost per Watt: <10 cents/W
- Design Cycle from Spec to Volume Production: < 8 Months

Facility Power System with 380-V DC Distribution Bus



This new emerging DC Bus approach sets very demanding requirements to Dc-Dc Transformer

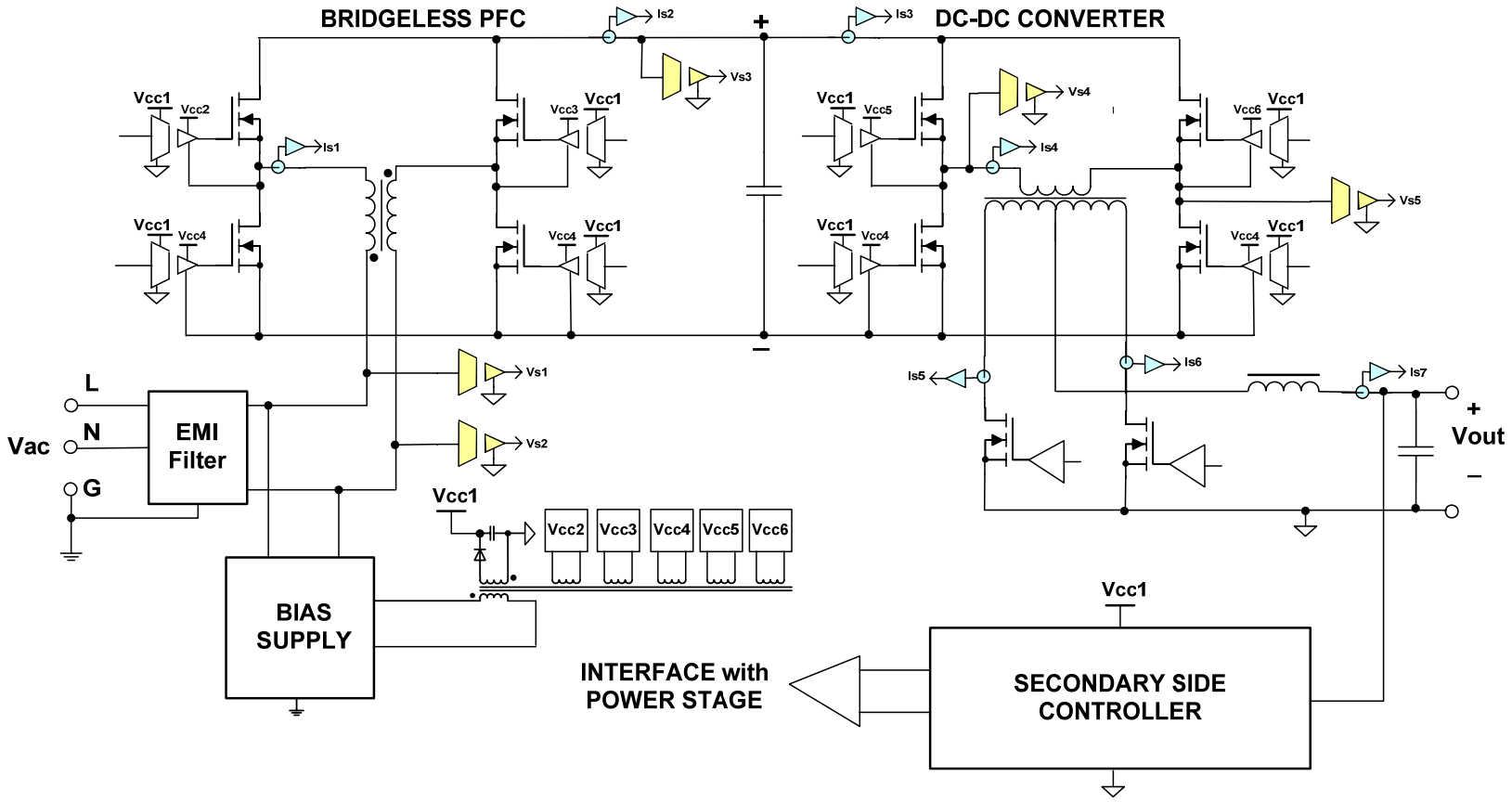
Design Goals for High input Dc-Dc Transformer



- Efficiency: >97% at half-load and 97% at full load
- Power Density: 300 W/cub.inch
- Cost per Watt: <12 cents/W
- Design Cycle from Spec to Volume Production: < 6 Months

The Need for Integration in Power System

AC/DC Concept Power Supply



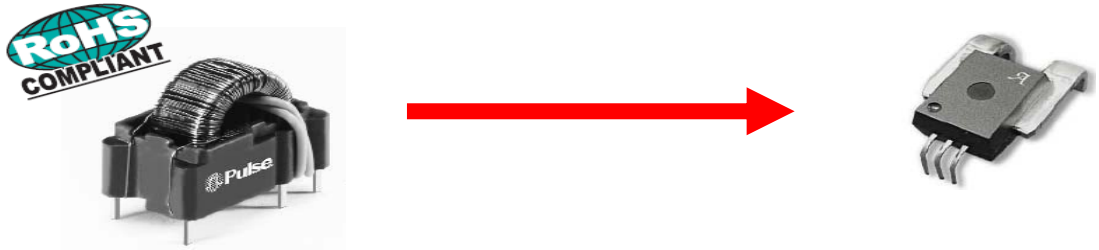
There are 8 drivers with safety insulation (10 overall), at least 4 current sensors with safety insulation (7 overall), 5 voltage sensors with safety insulation (6 overall), 6 isolated bias voltages and only 1 or 2 controllers in this power supply.

Some Integration Trends

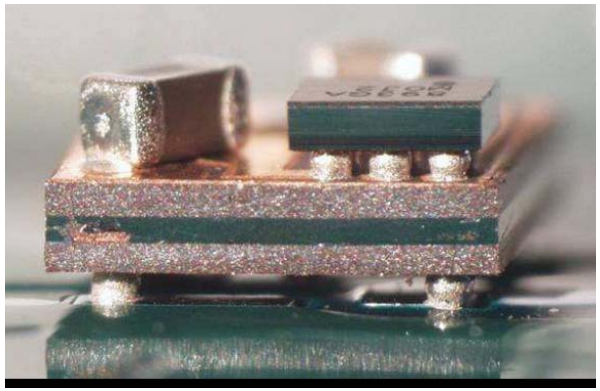
Integrated Isolated Bias Supply ICs for POL bias and isolation:

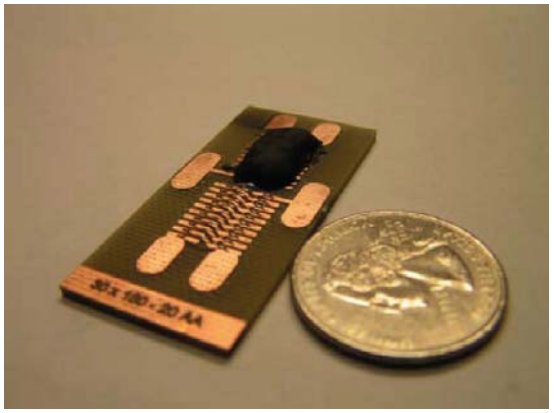
Fully isolated drivers with signal and bias isolation in package:

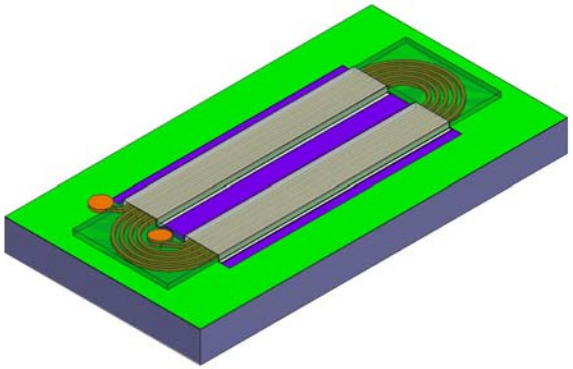
Isolated current, voltage and temperature sensing:



Target Spec for Micro-Magnetics used in PwrSoC







Micro-Inductor:

Size: 0402, 0603, 0805, 1206

Profile: <0.15 mm (without substrate)

Inductance: 20 to 200 nH

Frequency: 6 up to 100 MHz

Efficiency: 80% to 95%

Cost: $0.01 per sq. mm

Micro-Transformer:

Size: 0402, 0603, 0805, 1206

Profile: <0.1 mm (without substrate)

Inductance: 100 to 300 nH

Frequency: 10 up to 30 MHz

Efficiency: 70% to 90%

Cost: $0.01 per sq. mm

Power: 0.5 to 1.0W

Isolation: up to 3kV rms

Conclusion

- There is strong motivation for PSiP and PwrSoC approach even in high current and power systems
- In Case 1 of powering large scale digital processors, PwrSoC approach allows reduce the number of external decoupling capacitors and improve transient response
- In Case 2 of Data Communication Power System, PwrSoC approach applied to bias supplies, driver ICs and current/voltage sensing allows increase efficiency and power density, reduce time to market